Practice problems

Problem 1

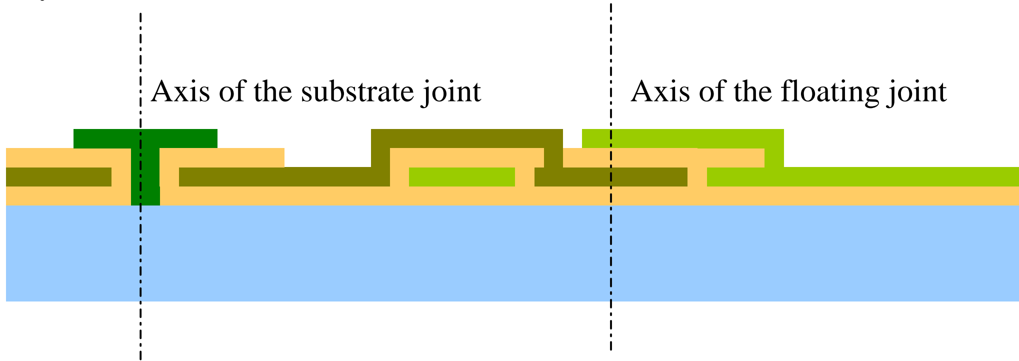
Consider the two-level surface micromachining process consisting of the following steps:

- Silicon dioxide layer 1 over the single crystal silicon substrate
- Patterning of the oxide layer
- Conformal deposit of polysilicon 1 layer
- Patterning of poly 1 layer
- Conformal deposit of oxide 2 layer
- Patterning of oxide 2 layer
- Conformal deposit of poly 2 layer
- Patterning of poly 2 layer
- Sacrifice of oxide layers 1 and 2

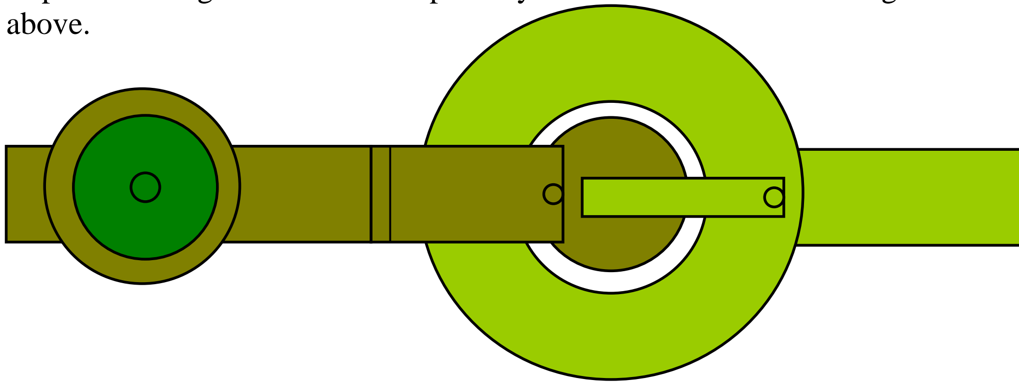
You have seen how a "substrate-hinge" with the axis of rotation vertical to the plane of the wafer can be made with this process. Now, create a "floating-hinge: with axis parallel to that of the substrate hinge. Please submit mask drawings as well as some 3-D drawings of the created hinge to convey your idea clearly. Cardboard or origami models are also fine in lieu of 3-D drawings/sketches. Remember that the hinge you create should not fall off when you flip it up side down.

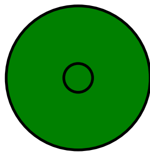
If you solve this problem without looking at the solution that is given in the next page, you can feel confident that you have understood the complexity of the geometric design of surface-micromachined mechanical devices.

In-plane substrate and floating joints using only two structural layers and two sacrificial layers.



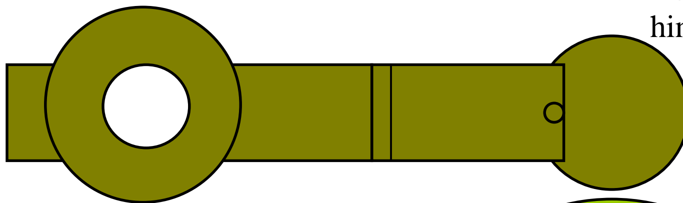
Top views – together and then separately below with colors matching with the side view above.

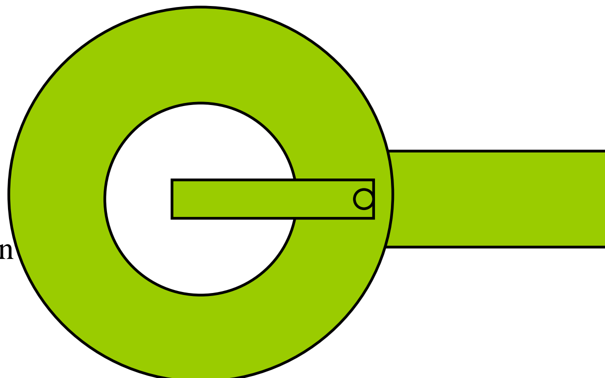




Hub of the substrate hinge

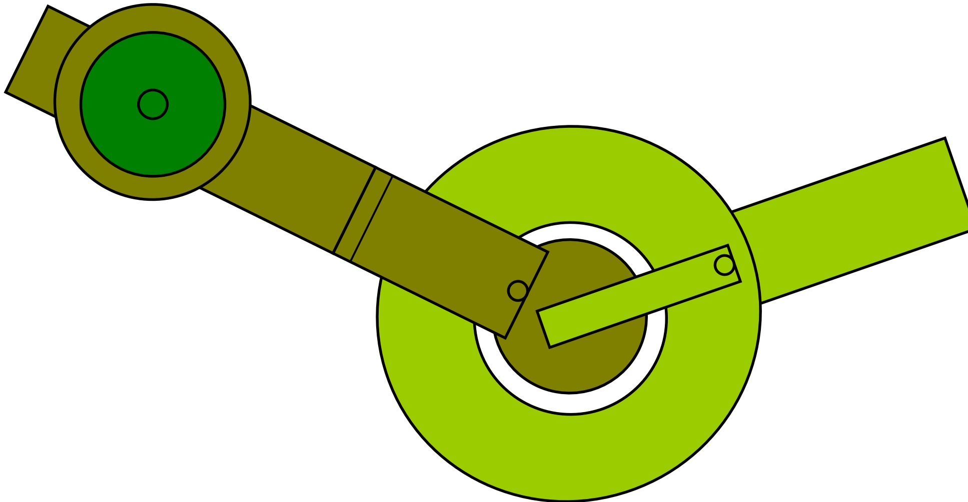
Body with substrate and floating hinges at the either end





Body with the floating hinge on one end

After rotation, the substrate and floating hinges look as follows.



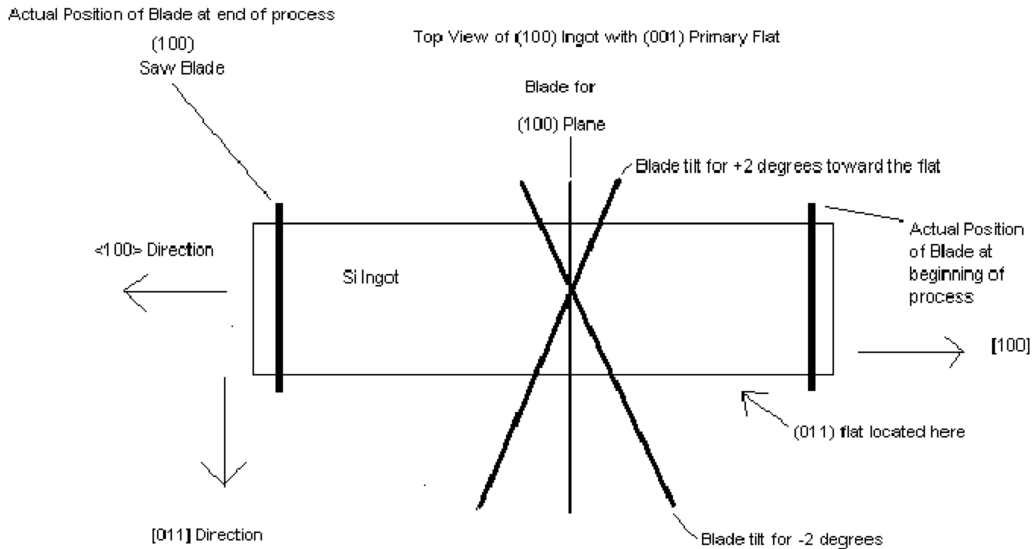
Problem 2

A (100) silicon wafer of thickness 300 um has a rectangular mask opening of 50 um × 200 um. The 200 um long edges are aligned with [110] direction. This wafer is subjected to DRIE so that a vertical trench of 100 um depth is first formed. Assume that the mask is intact during the DRIE process. The wafer is later wet-etched in KOH solution with the same mask in place for 30 minutes. Assume that the etch rate in [100] direction is 1.1 um/min and 1.6 um/min in the [110] direction. If you need etch rates on other planes, look into the literature. Sketch the cross-section of the resulting pit as seen in the plane formed by [110] and [100] vectors and passing through the middle of the rectangular opening. Mark all the exposed planes in this cross-section view.

First, we need to clarify the way the flat on (100) wafers is oriented. It is usually said that it is along the [110] direction. But a closer examination tells us that it is actually [011] direction. Since the choice of the coordinate system is arbitrary, [110] and [011] directions might mean the same direction for different peoples with different choices of coordinate frames. This causes some confusion. But to understand the KOH etching of (100) silicon as per the known results, the wafer flat is along [011] direction and the rectangle should be aligned with this direction.

For further clarity, consider how a (100) silicon ingot is cut to create the wafer flat before it is sliced to thin wafers (see Figure 2.1). Now, compare with the silicon crystal polyhedron. It is the [011] direction that actually lies parallel to the (100) plane and not the [110] direction. Thus, the rectangle of 200 um × 50 um is to be drawn at 45º to the square representing the (100) plane in the silicon crystal polyhedron with 200 um side oriented along the [011] direction.

Now, with this orientation, when we vertically go down with the DRIE etch, (011) planes get exposed rather than (010) planes. The etch rate along (011) planes is the same as that on the (110) planes because the choice of the coordinate system is arbitrary. The etch stops on (111) planes in both (100) and (011) oriented surfaces. So, the etch proceeds as shown in the figure below. The conformation is shown in the experimental evidence shown in Figure 2.3 where the KOH etch seems to be for much less time.



Slicing of (100) silicon wafers and the orientation of the primary flat in the [011] direction (from Virginia Semiconductor's website)

After DRIE… After KOH etching with the same mask…

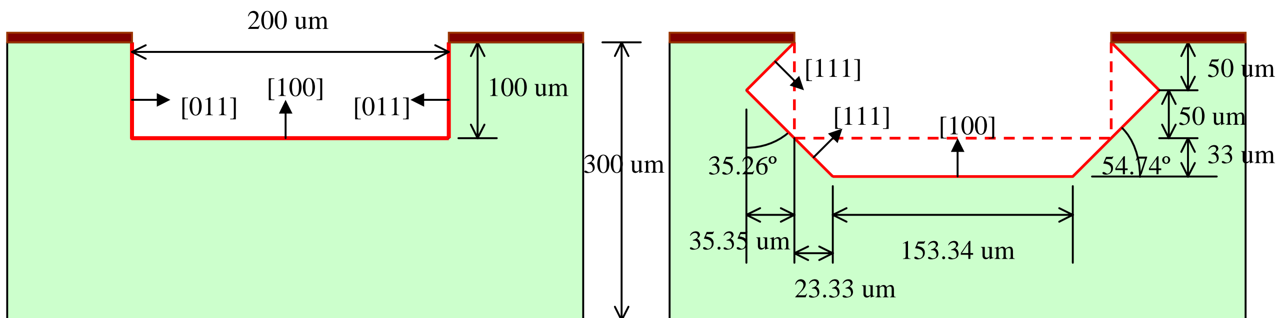


Figure 2.2 Cross-section profiles after DRIE and then KOH etch

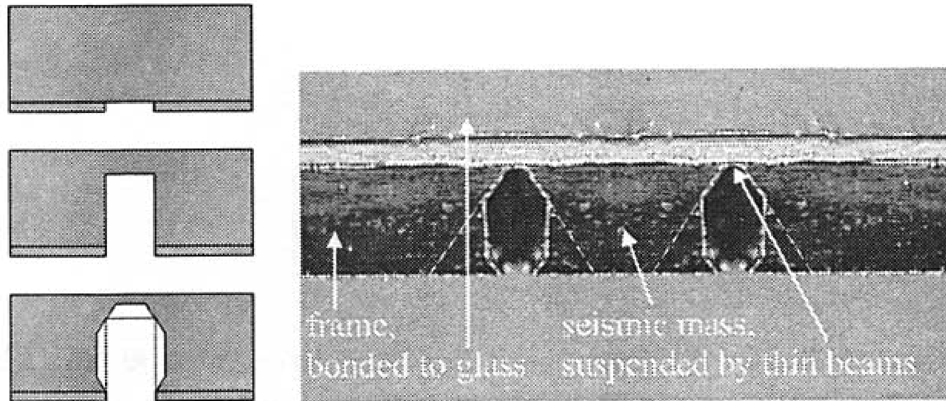


Figure 2.3 The experimentally observed cross-sections if the KOH is for a very short time (from Steve Reyntjens PhD thesis, K. U. Leuven)

Problem 3

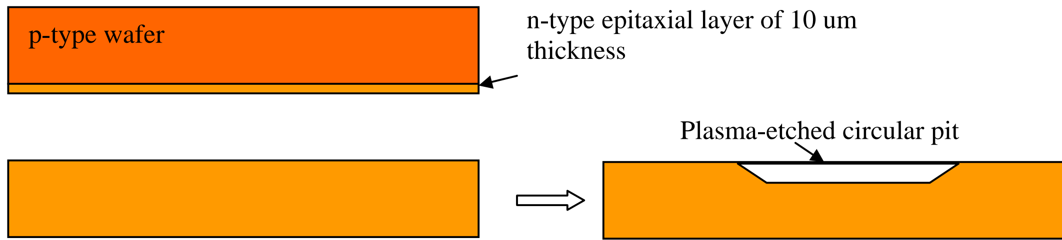
The cover of our textbook shows an image of the piezoresistive pressure sensor made at MIT using a "sealed-cavity" process developed there. Search the literature (IEEE Xplore is a good place to do it online. Try ieeexplore.ieee.org) to know more about this device and how it is made. Write a detailed verbal description of this process and sketch the step-by-step process flow. An extra credit of 5 points if you also draw the masks. The dimensions need not be exact and the mask drawings need not be to scale.

Sources:

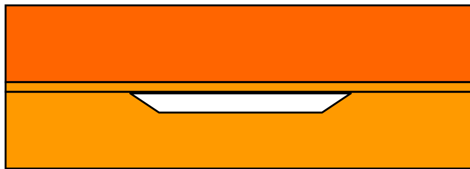
1) “A Merged MEMS-CMOS Process Using Silicon Wafer Bonding”, L. Parameshwaran, C. Hsu, and M. A. Schmidt, IEDM 95, pp. 613-616.

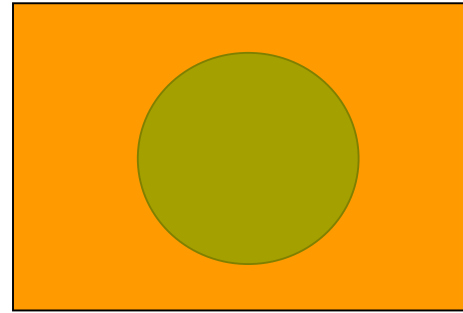
2) “Silicon Pressure Sensor Using A Wafer-Bonded Sealed-Cavity Process,” L. Parameshwaran, A. Mirza, W. K. Chan, and M. A. Schmidt, Transducers 95, pp. 582-585.

The process begins with two (100) oriented silicon wafers, one of p-type and another of n-type. A 10 um thick n-type layer is grown epitaxially on the p-type silicon wafer. A shallow circular pit is etched into the n-type silicon wafer using plasma etching. The two wafers are then cleaned and are brought into contact (the shallow pit on the n-type wafer is in contact with the n-type epi layer of the p-type wafer) and annealed at 1100 ºC for one hour. This enables the bonding of the two wafers. Next, the p-type wafer is thinned down by grinding and polishing, and then electrochemically etched so that the etch stops on the n-type epi layer. This leaves a circular membrane of uniform thickness of 10 um. At four locations along the periphery, U-shaped piezoresistors are formed by a masked doping (e.g., using ion implantation). A subsequent metallization step creates the electrical connections (e.g., using lift-off patterning). A hole is opened at the back using KOH for connecting to the pressure source and the device is packaged.

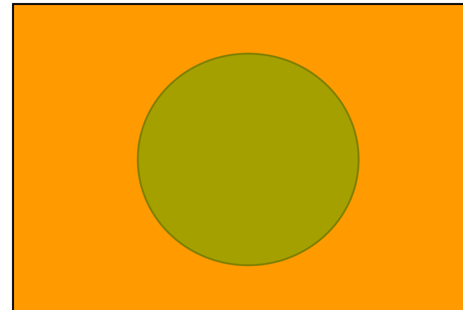


Wafer-to-wafer thermal bonding

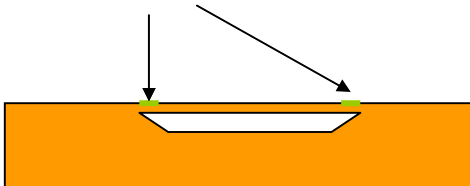


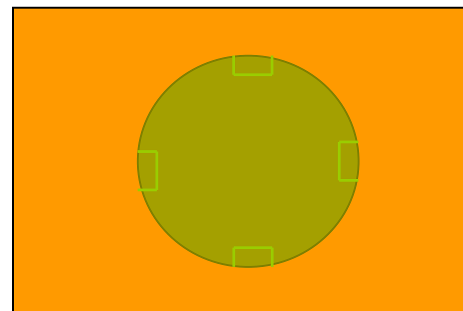


Grinding and polishing followed by electrochemical etching that stops on n-type layer

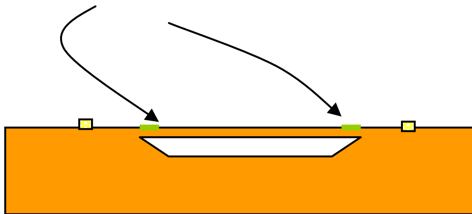


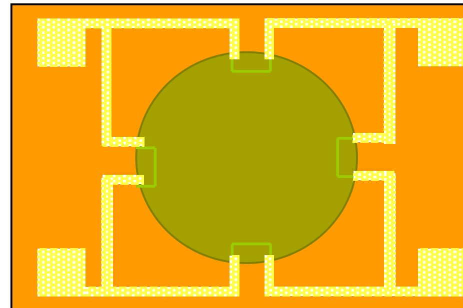
Implant piezoresistors using a mask



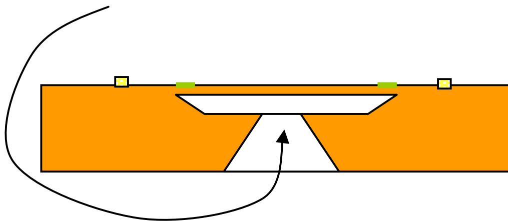


Metallization to define the electrical connections





KOH etching at the bottom to create an opening



Possible packaging