# ME – PhD Thesis Colloquium

## Statics and Dynamics of Connected Shallow Arches with Applications to Dynamically Offloading Footwear and Mechanical Logic Gates and Processors

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### ABSTRACT

The analytical and semi-analytical methods and criteria developed in this thesis for studying the nonlinear mechanics of connected shallow arches, which undergo snap-through or bistability, enable computationally efficient analysis and facilitate insightful design of arches for different applications.

The first design study considers person-specific dynamically offloading insoles for therapeutic footwear to ensure that plantar pressure stays below 200 kPa, reducing the risk of foot ulceration. This necessitated the study of dynamics of snapping arches under a time-varying load. We observed that an arch slows down as it switches from one stable state to the other. This delay in the switching increases as the applied force approaches the static critical force value. Dynamic analysis of arches enables us to exactly predict the switching force value of arches for a linearly varying time-dependent loading, which further helps us customize the insole based on person's walking speed. We prototyped such footwear and observed a maximum of 57% offloading at the forefoot region and 34% overall. To further increase the efficacy of the proposed self-offloading insole, we propose connected pinned-pinned arches where two arches of opposite curvature are joined together at a common pin joint. We computationally prove that this arch configuration is more effective as they not only help offload the high-pressure regions but also redistribute the pressure to other areas of the foot. We derive analytical criteria for bistability and flipping of connected arches. We also obtain a closed-form bilateral relationships that correlate the two stable state configurations of a connected arch.

Our second design study considers one of the simplest designs of mechanical logic gates and processors. Here, the total number of deformable parts or arches is limited to the total numbers of inputs and outputs required for a particular logic operation, e.g., for an AND gate or OR gate, we need only three connected pinned-pinned arches—two for the inputs and one for the output. Along with the AND gate and OR gate, we also propose Encoder and De-Multiplexer logic processors.


### ABOUT THE SPEAKER

Priyabrata Maharana is a PhD student in the Department of Mechanical Engineering, IISc, Bengaluru. He is working with Prof. G. K. Ananthasuresh in Multidisciplinary and Multiscale Design and Device (M2D2) laboratory. He completed BTech from GCE Kalahandi, Odisha, in 2014, and MTech from IIT-Guwahati in 2017. His research interests include compliant mechanisms, nonlinear dynamics, topology optimization, and biomedical device design.